

Appl. No. 10/801,455  
Amdt. dated December 14, 2005  
Reply to final Office action of September 19, 2005

AMENDMENTS TO THE SPECIFICATION

Please delete the text on page 4, beginning on line 1 of the third paragraph and ending at line 5 of the third paragraph, of the specification as indicated below:

**Specification Text:**

current for biasing the D flip-flop, wherein the one of at least two current is receivable from an on-chip biasing current source and the other of the one of at least two current is receivable from a constant biasing source, according to a first aspect of the invention.

In accordance with a second aspect of the invention, there is disclosed a method for performing biasing current selection, the method comprising the steps of applying a first current to an input terminal of a first receiving means and a second current to an input terminal of a second receiving means. Providing the first current from an output terminal of the first receiving mean and the second current from an output terminal of the second receiving means. Summing the first current and the second current to produce a summed current at a summing node. Comparing the summed current with the second current by a current comparator and selecting one of the first current and the second current as an output current by the current comparator in response to the summed current and the second current being compared.

~~In accordance with a third aspect of the invention, there is disclosed a current selective D flip-flop circuit capable of performing biasing current selection, the current selective D flip-flop circuit comprises a D flip-flop, a current selector circuit coupleable to the D flip-flop and a current multiplier, wherein the current selector circuit is coupled to the D flip-flop through the current multiplier.~~

**Brief Description Of The Drawing**

Embodiments of the invention are described hereinafter with reference to the drawings, in which:

Fig. 1 is a prior art schematic diagram of a current-mode D flip-flop;

Fig. 2 is a schematic diagram of a current selector circuit according to an embodiment of the invention;